LAW OFFICES
LEYDIG, VOIT & MAYER, PROFESSIONAL CORPORATION
700 THIRTEENTH ST., N.W., SUITE 300
WASHINGTON, D.C. 20005-3960

TELEPHONE: (202) 737-6770 FACSIMILE: (202) 737-6776

FACSIMILE COVER SHEET

DATE: AUGUST 23, 2005

NUMBER OF PAGES (INCLUDING THIS TRANSMITTAL COVER SHEET): 6

OUR REFERENCE: 401191

FROM: Jeffrey A. Wyand
REGISTRATION NO. 29,458
(202) 737-6770 Ext. 219

TO: EXAMINER D. TON
GROUP 2133
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C.

TELEPHONE NUMBER:
FACSIMILE NUMBER: 571 273 8300

IN RE APPLN. OF:	HATAKENAKA ET AL.
SERIAL NO.	09/871,978
FILED:	JUNE 4, 2001
FOR:	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE COMPRISING RAM WITH COMMAND DECODE SYSTEM AND LOGIC CIRCUIT INTEGRATED INTO A SINGLE CHIP AND TESTING METHOD OF THE RAM WITH COMMAND DECODE SYSTEM
GROUP ART UNIT:	2133
EXAMINER:	D. TON

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application No. 09/871,978

Applicant: HATAKENAKA et al.

Filed: June 4, 2001

TC/AU: 2133

Examiner: D. Ton

Docket No.: 401191

Customer No.: 23548

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

LETTER TRANSMITTING SUPPLEMENTAL DECLARATION

Sir:

Further to the recently mailed Interview Summary, Applicants now submit a Supplemental Declaration regarding the most recent amendments in the re-issue patent application.

Entry of the Supplemental Declaration and prompt issuance of the Notice of Allowance are respectfully requested.

Respectfully submitted,

Jeffrey A. Wyand, Reg. No. 29,458
LEYDIG, VOIT & MAYER
700 Thirteenth Street, N.W., Suite 300
Washington, DC 20005-3960
(202) 737-6770 (telephone)
(202) 737-6776 (facsimile)

Date: August 23, 2005
JAW:ves

5040950502
G062US02

SUPPLEMENTAL DECLARATION

As a below-named inventor, I declare that:

my residence, post office address, and citizenship are as stated next to my name;

I believe that I am an original and first inventor of the invention entitled "Semiconductor Integrated Circuit Device Comprising Synchronous DRAM Core And Logic Circuit Integrated Into A Single Chip And Method Of Testing The Synchronous DRAM Core" described and claimed in the specification of U.S. Patent Application No. 09/871,978, filed June 4, 2001, which is an application for re-issue of U.S. Patent 5,910,181;

I have reviewed and understand the contents of the specification, including the claims, as amended by the Preliminary Amendment filed June 4, 2001 and the Amendments filed December 31, 2003 and June 14 2004;

I acknowledge the duty to disclose information that is material to the examination of this application in accordance with 37 C.F.R. §1.56(n); and

I hereby claim foreign priority benefits under Title 35, United States Code §119 of the foreign application for patent listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application from which the benefit of priority is claimed.

Prior Foreign Application

(Number)	(Country)	(Day/Month/Year Filed)
9-086600	Japan	04/04/97

United States Patent 5,910,181, which matured from United States Patent Application Serial Number 08/964,236, is partly inoperative or invalid by reason of claiming both less and more than I had a right to claim based on the disclosure of the patent application. The patent application disclosure does not limit the invention to a synchronous dynamic random access memory but discloses the invention as pertaining to other kinds of random access memories, particularly as described at column 13, lines 62-65 of United States Patent 5,910,181. This aspect of the invention is encompassed by my re-issue claims 10-16. In addition, minor errors of a grammatical or typographical nature and potential antecedent issues appear in claims 1-7, and 9 of U. S. Patent 5,910,181. Claims 7 and 8 may have been broader than permissible in view of the prior art.

To the best of my knowledge, the errors occurred without deceptive intent. Correction of the errors is sought by correcting claims 1-3, 5, 6, and 7, and by adding claims 10-16 as shown in the Amendment filed June 14, 2004. In that Amendment,

In re Appln. of Hatakenaka et al.
Application No. 09/871,978

claims 7 and 9 of U.S. Patent 5,910,181 were combined as claim 7 and claims 8 and 9 were cancelled as inconsistent with amended claim 7.

In re Appln. of Hatakenaka et al.
Application No. 09/871,978

As a named inventor, I hereby appoint Leydig, Voit & Mayer to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Customer Number 23548.

23548

I further direct that correspondence concerning this application be directed to Leydig, Voit & Mayer: Customer Number 23548.

23548

I declare that all statements made here based on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of this reissue patent application or any reissued patent issuing from this application.

Full name of first joint inventor: Makoto HATAKENAKA

Inventor's signature Makoto Hatakenaka

Date July 5, 2005 Country of Citizenship: Japan

Residence: Tokyo, Japan
(city/state or country)

Post Office Address: c/o Renesas Technology Corp., 4-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-6334, Japan

Full name of second joint inventor: Akira YAMAZAKI

Inventor's signature Akira Yamazaki

Date July 29, 2005 Country of Citizenship: Japan

Residence: Tokyo, Japan
(city/state or country)

Post Office Address: c/o Renesas Technology Corp., 4-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-6334, Japan

504095US02
G0621US02

Full name of **third joint inventor**, if any: Shigeki TOMISHIMA

Inventor's signature Shigeki Tomishima

Date Aug. 10, 2005 Country of Citizenship: Japan

Residence: Tokyo, Japan
(city/state or country)

Post Office Address: c/o Mitsubishi Denki Kabushiki Kaisha, 2-3, Marunouchi 2-Chome, Chiyoda-ku, TOKYO 100-8310 JAPAN

Full name of **fourth joint inventor**, if any: Tadato YAMAGATA

Inventor's signature Tadato Yamagata

Date July 7, 2005 Country of Citizenship: Japan

Residence: Tokyo, Japan
(city/state or country)

Post Office Address: c/o Renesas Technology Corp., 4-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-6334, Japan